MC33567

Dual Linear Controller for High Current Voltage Regulation

The MC33567 Dual Linear Power Supply Controller is designed to facilitate power management for motherboard applications where reliable regulation of high current supply planes is required. It provides the Drive, Sense and Control signals to interface two external, N−channel MOSFETs for regulating two different supply planes. Undervoltage short circuit detection places the operation of the system into a protected mode pending removal of the short.

Features

- Two Independent Regulated Supplies
- MC33567−1: 1.515 V − Supply for GTL and AGP Planes
  1.818 V − Supply for I/O Plane and Memory Termination
- MC33567−2: Dual 2.525 V Supplies for Clock and Memory
- MC33567−3: 2.3 V − Voltage Supply
  1.2 V − Voltage Supply
- Undervoltage Short Circuit Protection
- Supply Undervoltage Detection
- Drive Capability for N−Channel MOSFETs
- Bypass Function for 3.3 V AGP Card Detection
- Pb−Free Package May be Available. The G−Suffix Denotes a Pb−Free Lead Finish

Applications

- Motherboards
- Dual Power Supplies

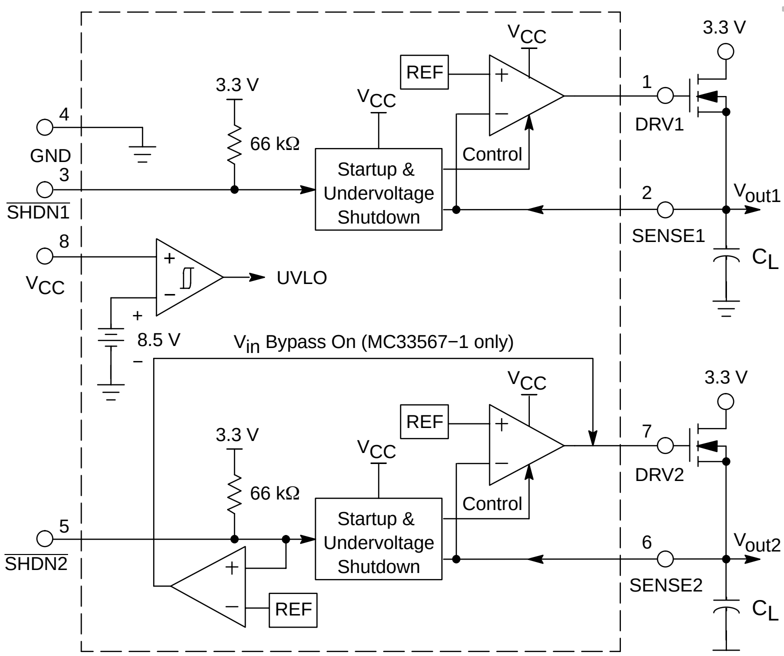
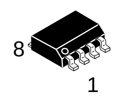


Figure 1. Simplified Block Diagram

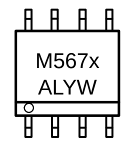
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

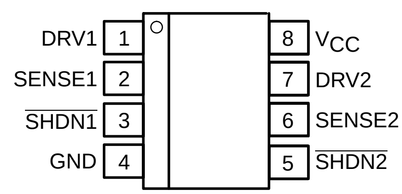


SO−8
D SUFFIX
CASE 751



x = 1, 2 or 3
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

PIN ASSIGNMENTS AND FUNCTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	DRV1	Gate 1 drive. Is internally clamped to ground in power down mode.
2	SENSE1	Sense 1 line. Sense load voltage and provides feedback to regulator.
3	$\overline{SHDN1}$	TTL high level turns on regulation for gate 1. (Internal pull−up to 3.3 V)
4	GND	
5	$\overline{SHDN2}$	TTL high level turns on regulation for gate 2. (Internal pull−up to 3.3 V)
6	SENSE2	Sense 2 line. Sense load voltage and provides feedback to regulator.
7	DRV2	Gate 2 drive. Saturates external FET in bypass mode (MC33567−1 only). Is internally clamped to ground in power down mode.
8	V_{CC}	Supply voltage for operation and gate drive output − typically 12 V.

MAXIMUM RATINGS (Notes 1, 2 and 3)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	12.5	Vdc
$\overline{\text{SHUTDOWN}}$ Voltage	$V_{\overline{SHDN}}$	V_{CC}	Vdc
Operating Ambient Temperature	T_A	0 to 80	°C
Operating Junction Temperature	T_J	−5.0 to 125	°C
Lead Temperature (Soldering, 10 seconds)	T_L	300	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ (Note 2)	159	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	28	°C/W

1. ESD Ratings
   ESD Machine Model protection up to 200 V, class B.
   ESD Human Body Model protection up to 2000 V, class 2.
2. Minimum pad test board with 5 MIL wide and 2.8 MIL thick copper traces1 inch long.
3. All characterizing done with MTD3055VL N−Channel MOSFETs.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, $V_{\overline{SHDN}1} = V_{\overline{SHDN}2}$ = 2.0 V, T_A = 0°C to 80°C, typical values shown are for T_J = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{cc}	9.0	12	12.5	V
Quiescent Current — $V_{\overline{SHDN}1} = V_{\overline{SHDN}2}$ = 0 V $V_{\overline{SHDN}1} = V_{\overline{SHDN}2}$ = 2.0 V	I_{qL} I_{qH}	− −	5.8 6.3	9.0 10	mA
UNDERVOLTAGE LOCKOUT					
Undervoltage Lockout Threshold Voltage (V_{CC} Increasing)	UVLO	7.0	8.5	9.0	V
Hysteresis Voltage (V_{CC} Decreasing)	$UVLO_{Vhys}$	0.2	0.5	0.9	V
DRIVE OUTPUTS					
Drive Output Voltage (Gate to Ground)	V_{drv}	−	10.5	−	V
Drive Output Source Current (T_J = 25°C)	I_{pkdrv}	10	20	30	mA
Gate Drive Output Sink Current (V_{sense} = 0 V, T_J = 25°C)	I_{sink}	4.0	7.0	10	mA
$\overline{\text{SHUTDOWN}}$ INPUTS					
Shutdown Threshold Voltage (Drive output on to off, ramp $V_{\overline{SHDN}}$ to 0 V)	$\overline{SHDN}_{Vth}$	0.8	1.13	1.3	V
Shutdown Threshold Hysteresis (Drive output off to on)	$\overline{SHDN}_{hys}$	50	130	200	mV
Shutdown Disable Time (Drive output on to off, ramp $V_{\overline{SHDN}}$ to 0 V)	$\overline{SHDN}_{tdis}$	−	0.5	2.0	μs
Shutdown Input Current ($V_{\overline{SHDN}}$ = 0 V)	$I_{\overline{SHDN}}$	−	−50	−	μA
SHORT CIRCUIT					
Short Circuit/Undervoltage Detect Threshold (Load current increased until output voltage drops activating hiccup mode)	SC_{uvd}	70	75	80	%Vout
Drive Output Response Time to short circuit (Ramp down V_{sense} to 0 V)	SC_{td}	200	325	500	μs
Drive Output On Time in hiccup mode (V_{sense} = 0 V)	SC_{ton}	0.5	0.97	1.5	ms
Drive Output Off Time in hiccup mode (V_{sense} = 0 V)	SC_{toff}	20	47.7	60	ms
OUTPUT REGULATION					
Regulator Output Voltage (V_{in} = 3.3 V, I_L = 5.0 mA to 1.3 A)					V
MC33567−1 Output 1	V_{out1}	1.773	1.818	1.864	
Output 2	V_{out2}	1.477	1.515	1.553	
MC33567−2 Output 1	V_{out1}	2.462	2.525	2.589	
Output 2	V_{out2}	2.462	2.525	2.589	
MC33567−3 Output 1	V_{out1}	2.243	2.300	2.358	
Output 2	V_{out2}	1.170	1.200	1.230	
Output Voltage Regulation (I_L = 5.0 mA to 1.3 A)	$V_{reg\%}$	−2.5	−	+2.5	%

OPERATING DESCRIPTION

Introduction

The MC33567 series is a family of Dual Linear FET Controllers designed for Power Management applications where high current, voltage regulation is needed. Some computer applications include:

- 1.2 V − Power Supply
- 1.515 V − AGP (Advanced Graphic Port) and GTL+ (Gunning Transistor Logic − Intel's electrical bus technology)
- 1.818 V − I/O planes on motherboards
- 2.3 V − Power Supply
- 2.525 V − Clock and memory

The MC33567 provides tight output voltage regulation, (V_{out}), and incorporates individual $\overline{SHDN}$ controls for each FET controller and voltage protection by sensing the output voltage.

Output:

The MC33567 provides tight output voltage regulation from one or two supply voltages using 2 external N−Channel MOSFETs. Each controller operates independently and regulates the output voltage to a predetermined level (1.2 V, 1.515 V 1.818 V, 2.3 V or 2.525 V). In addition, regulator 2 of the MC33567−1 incorporates a V_{in} bypass mode on which the external FET is fully enhanced.

Shutdown:

The regulated outputs of the MC33567 can be disabled with the use of the $\overline{SHDN}$ pin. It also determines the output voltage level. $\overline{SHDN}$ can be controlled externally from board signals like the AGP or GTL+ as shown in Figure 3.

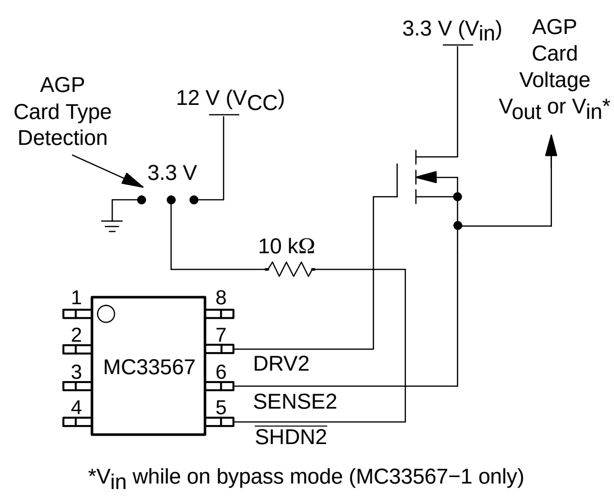


Figure 3. 1.5 V/3.3 V AGP Card Detection

Listed below are the $\overline{SHDN}$ threshold voltage levels and the corresponding regulator output voltages:

1. If the $\overline{SHDN}$ pin is left open, the output voltage is set to its regulated value.
2. If a voltage less than 0.8 V is applied to the $\overline{SHDN}$ pin, the output voltage is set to 0 V.
3. If a voltage greater than 1.3 V and less than 4.1 V is applied to the $\overline{SHDN}$ pin, the output voltage is set to its regulated voltage.
4. If the $\overline{SHDN}$ voltage is pulled above 4.1 V, the MC33567 enters a V_{in} bypass mode. In this mode, the MOSFET is fully enhanced and the output voltage is the MOSFET drain voltage (V_{in}) minus the MOSFET drain−source on voltage $V_{DS(on)}$. This feature is only available on REGULATOR 2 of the MC33567−1.

Table 1 summarizes the output voltage options and its relationship with $V_{\overline{SHDN}}$.

Table 1. Logic Table for $\overline{SHDN}$ Pin

Device	$V_{\overline{SHDN}}$ (V)	V_{out} (V)
MC33567−1		
REGULATOR 1	No Connect	1.818 V
	< 0.8 V	0 V
	> 1.3 V	1.818 V
REGULATOR 2	No Connect	1.515 V
	< 0.8 V	0 V
	1.3 V < $V_{\overline{SHDN}}$ < 4.1 V	1.515 V
	> 4.1 V	$V_{in}-V_{DS(on)}$ (Bypass Mode)
MC33567−2		
REGULATOR 1 & REGULATOR 2	No Connect	2.525 V
	< 0.8 V	0 V
	> 1.3 V	2.525 V
MC33567−3		
REGULATOR 1	No Connect	2.3 V
	< 0.8 V	0 V
	> 1.3 V	2.3 V
REGULATOR 2	No Connect	1.2 V
	< 0.8 V	0 V
	> 1.3 V	1.2 V

Undervoltage Detection:

If V_{out} drops below 75% of the regulated threshold for greater than 250 μs or a short circuit condition is present, that output will go into short circuit or Hiccup Mode. While in Hiccup mode, the output is turned ON for 1.0 ms and OFF for 40 ms for a duty cycle of 1:41 as shown in Figure 4. This mode will continue as long as the fault is present. Once the fault is removed, the regulator will resume normal operation.

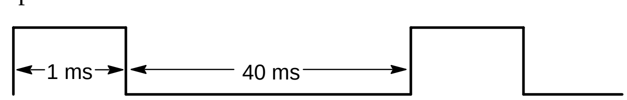


Figure 4. Hiccup Mode Duty Cycle

Sense:

If the load is located away from the regulator, the voltage drop on the connecting cable or trace can become significant. The MC33567 provides tight voltage load regulation with varying load currents using it's SENSE feature. As shown in Figure 5, the MC33567 senses the voltage at the load and provides feedback to the regulator. The regulator voltage is then adjusted to compensate for the load changes. It is recommended that the SENSE connection be placed as close as possible to the load. Also, use a separate trace to connect the source of the N−channel MOSFET to the load to avoid interference or coupling with the SENSE signal. The use of the SENSE feature is required for correct device operation. If the SENSE pin is not connected to the load, the output will go into Hiccup mode.

The current into the SENSE pin is given by the following equation:

$$I_{SENSE} = 100\ \mu A + \frac{V_{out}}{1.8\ k\Omega}$$

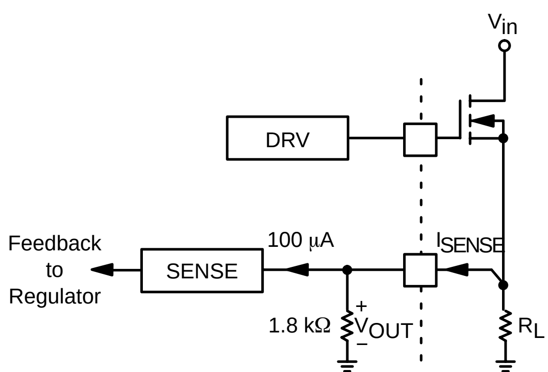


Figure 5. Voltage Regulation Using Sense Feature

N−Channel MOSFET Selection:

The MC33567 was characterized using ON Semiconductor's MTD3055VL N−channel MOSFET. Other MOSFETs can be used with the MC33567 as long as power and stability requirements are met.

Power:

A MOSFET with a low drain−source on resistance ($R_{DS(on)}$) will insure the output voltage is not drastically reduced due to excessive voltage drop across the MOSFET. The required $R_{DS(on)}$ can be calculated using the equation below:

$$R_{DS(on)} \le 0.5\ \frac{V_{in} - V_{out}}{I_{LOAD}}$$

where:

V_{in} = Input Voltage, typically 3.3 V
V_{out} = Regulator Output Voltage (1.2 V, 1.515 V, 1.818 V, 2.3 V, or 2.525 V)
I_{LOAD} = Load Current

A safety margin of 0.5 was added to account for $R_{DS(on)}$ variations over the operating temperature range.

Stability:

After evaluating the regulator, driver and load system using control theory it is demonstrated that the output capacitor, external driver gain and error amplifier gain bandwidth play an important role on the system stability. To insure system stability the following set of design guidelines should be followed:

$$C_i = C_{gs} + C_{gd}$$

$$\omega_f = \frac{1}{C_i \cdot R_o}$$

$$\omega_p = \left(\frac{1}{\omega_1} + \frac{1}{\omega_f}\right)^{-1}$$

$$\frac{1}{20 \cdot \left(1 + \frac{\omega_a}{(3 \cdot \omega_p)}\right)} \cdot \frac{1}{g_m} \le R_s \le \frac{(3 \cdot \omega_p)}{\omega_a} \cdot \frac{1}{g_m}$$

$$C_o \cdot R_s \ge 5 \cdot \left(\frac{1}{\omega_a} + \frac{1}{\omega_p}\right)$$

where:

ω_f = Driver pole frequency
C_i = Input and reverse transfer capacitance when device is off
R_o = Regulator output resistance (50 Ω for the MC33567)
ω_p = Secondary pole for open loop
ω_a = Error amplifier gain bandwidth
ω_1 = Error amp second pole (set $\omega_1 = \omega_a$, if not specified)
R_s = Output capacitor ESR
g_m = Maximum driver transconductance gain
C_o = Output capacitance
T = Overall loop response time

The output capacitor capacitance and ESR required for using the MTD3055VL as external driver are calculated as follows:

$$\omega_f = \frac{1}{C_i \cdot R_o} = \frac{1}{(1240\ pF + 600\ pF) \cdot (50\ \Omega)} = 10.87\ MHz$$

$$\omega_p = \left(\frac{1}{\omega_1} + \frac{1}{\omega_f}\right)^{-1} = \left(\frac{1}{5\ MHz} + \frac{1}{10.87\ MHz}\right)^{-1}$$

$$= 3.42\ MHz$$

$$\frac{1}{20 \cdot \left(1 + \frac{\omega_a}{(3 \cdot \omega_p)}\right)} \cdot \frac{1}{g_m} \le R_S \le \frac{(3 \cdot \omega_p)}{\omega_a} \cdot \frac{1}{g_m}$$

$$\frac{1}{20 \cdot \left(1 + \frac{5\ MHz}{(3 \cdot 3.42\ MHz)}\right)} \cdot \frac{1}{8.8\ mhos} \le R_S \le \frac{(3 \cdot 3.42\ MHz)}{5\ MHz} \cdot \frac{1}{8.8\ mhos}$$

$$3.8\ m\Omega \le R_S \le 233.2\ m\Omega$$

selecting an ESR of 30 mΩ, we have:

$$C_o \ge \frac{5}{R_S} \cdot \left(\frac{1}{\omega_a} + \frac{1}{\omega_p}\right)$$

$$C_o \ge \frac{5}{30\ m\Omega} \cdot \left(\frac{1}{5\ MHz} + \frac{1}{3.42\ MHz}\right)$$

$$C_o \ge 82.07\ \mu F$$

100 μF is selected as it is an industry standard value. Please note that if the system is designed to work with several drivers, the system has to be designed around the driver with higher gain to insure stability for all of them.

The design guidelines discussed in this section are conservative enough that satisfactory results may be obtained with devices that lie just outside of these guidelines, although deviation from these guidelines will generally cause instability. For a more detailed analysis on linear regulators stability please refer to ON Semiconductor application note AND8037/D.

Adjustable Output Voltage:

The MC33567 will regulate V_{out} to its preset voltage level, referenced at the sense pin. However, other V_{out} levels can be obtained scaling the sense voltage. This is done using a resistive network between the load and the sense pin as shown in Figure 6.

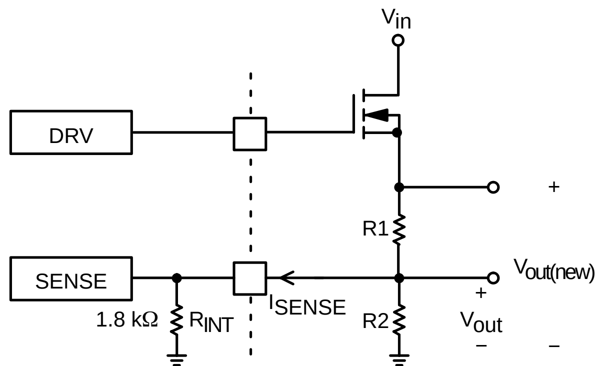


Figure 6. Output Voltage Scaling Using Resistive Network

The regulator will increase the load voltage until the SENSE pin voltage reaches the regulator voltage level, V_{out}. The new output voltage, $V_{out(new)}$, is calculated as follows:

$$V_{out(new)} = V_{out} + R_1 * \left(\frac{V_{out}}{R_2} + I_{SENSE}\right)$$

Please note that in this configuration R_2 and the sense internal resistor are in parallel. The parallel combination will reduce the effective resistance of R_2. If R_2 is in the range of R_{INT}, the parallel combination will be almost half of the original intended value of R_2. This will cause $V_{out(new)}$ to be smaller than calculated using the above equation. This is avoided making R_2 as small as possible, probably in the range of 10 to 50 Ohms. $V_{out(new)}$ is limited by the external driver drain current and its required Gate−Source voltage as well as the Drive Output Voltage, V_{drv}.

PCB Layout Guidelines

It is recommended that the MC33567 be placed as physically close as possible to the external series pass MOSFET transistors. Use short traces to minimize extraneous signals from being induced on the SENSE or DRV line. Also, avoid routing the SENSE line near the load and input current path, as well as the GND return current path to prevent signal coupling.

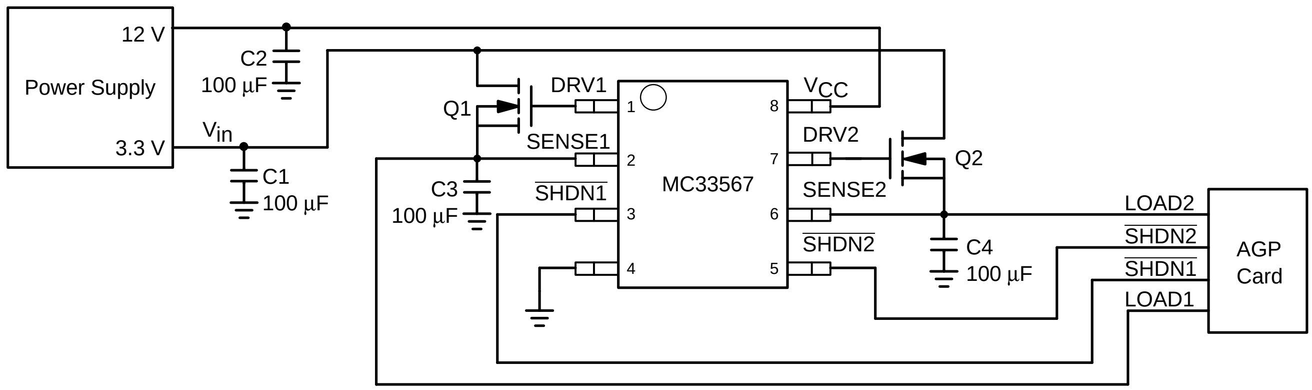


Figure 7. Application Block Diagram

Parts List

Qty	Reference	Part/Description	Vendor	Notes
4	C1, C2, C3, C4	100 µF Electrolytic Capacitor	Various	
1	U1	MC33567	ON Semiconductor	
2	Q1, Q2	MTD3055VL	ON Semiconductor	N−Channel MOSFET

MC33567 TYPICAL CHARACTERISTICS

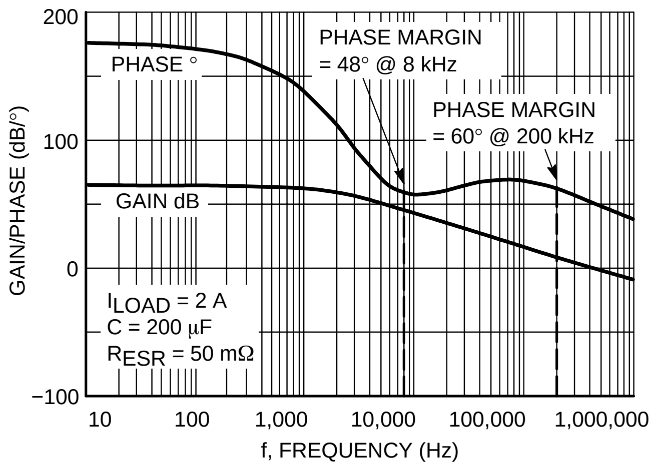


Figure 8. Gain−Phase Plot for Output Capacitor with 50 mΩ ESR

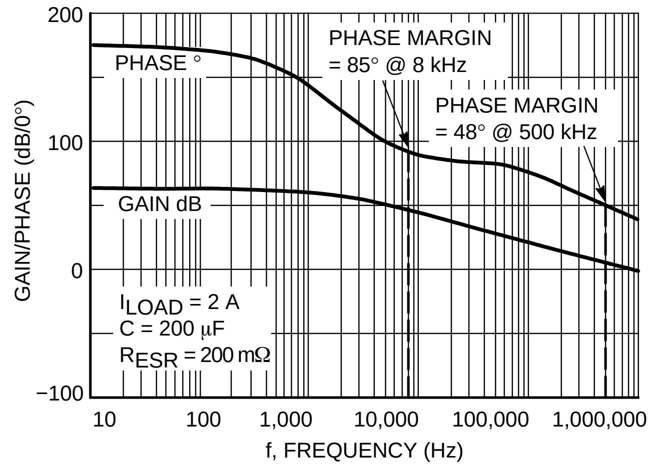


Figure 9. Gain−Phase Plot for Output Capacitor with 200 mΩ ESR

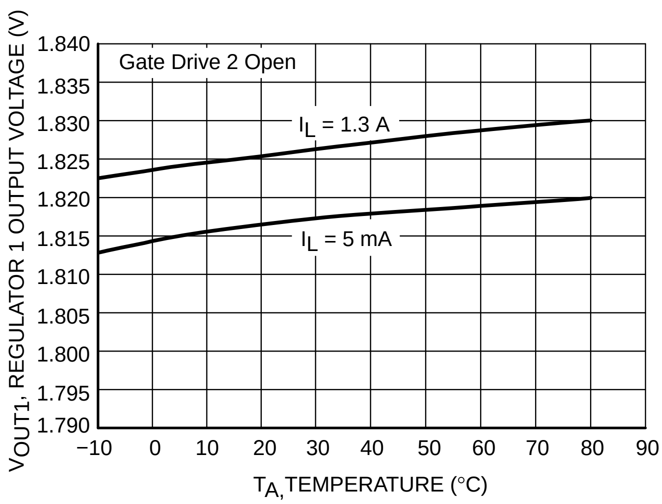


Figure 10. Regulator 1 (Suffix 1) Output Voltage vs. Ambient Temperature

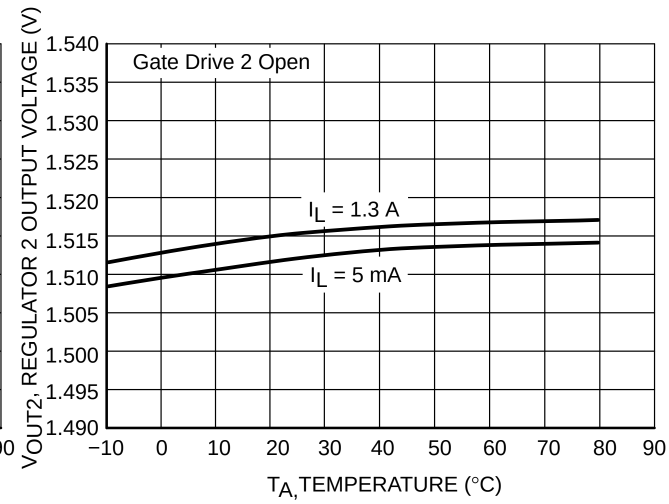


Figure 11. Regulator 2 (Suffix 1) Output Voltage vs. Ambient Temperature

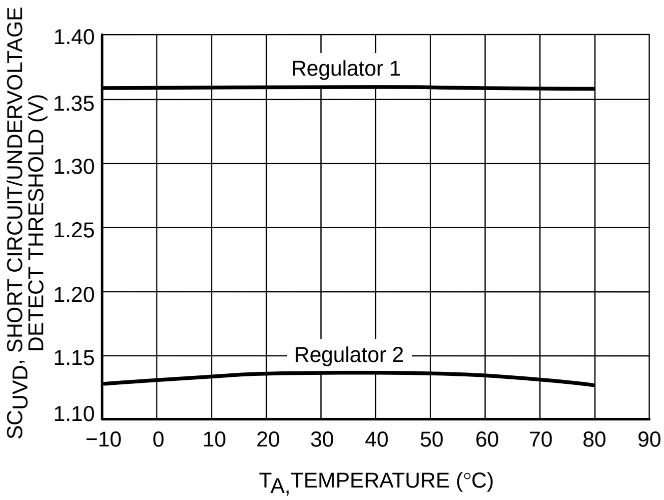


Figure 12. Short Circuit/Undervoltage Detect Threshold (Suffix 1) vs. Ambient Temperature

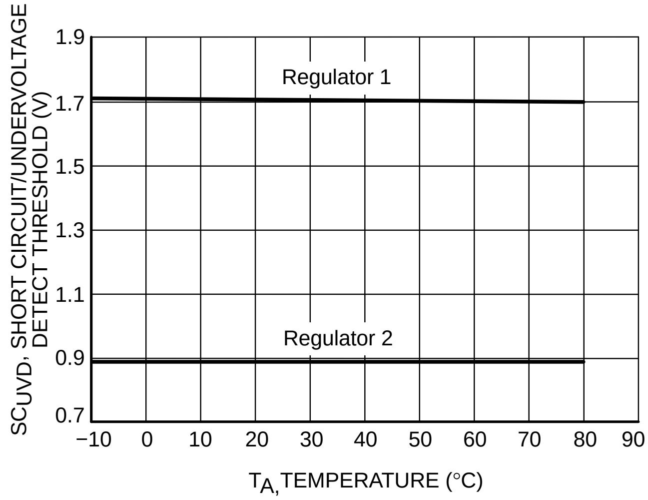


Figure 13. Short Circuit/Undervoltage Detect Threshold (Suffix 3) vs. Ambient Temperature

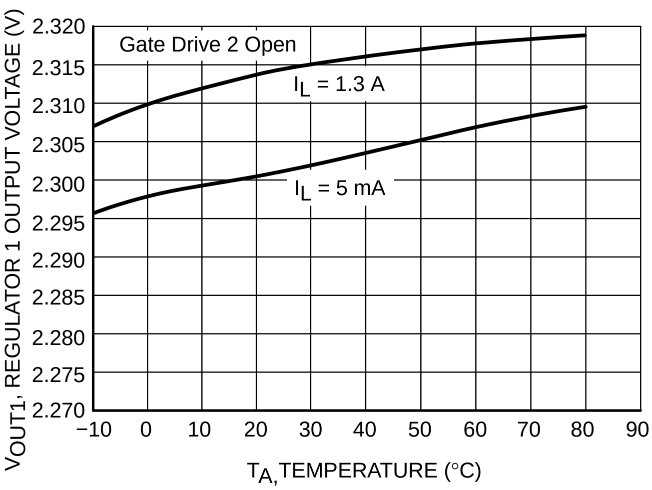


Figure 14. Regulator 1 (Suffix 3) Output Voltage vs. Ambient Temperature

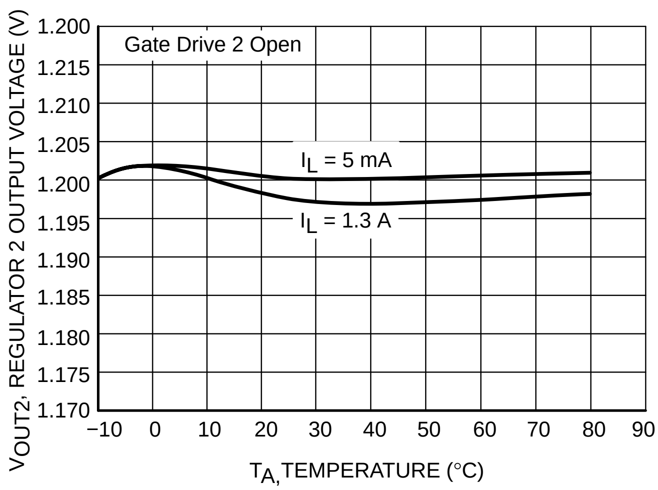


Figure 15. Regulator 2 (Suffix 3) Output Voltage vs. Ambient Temperature

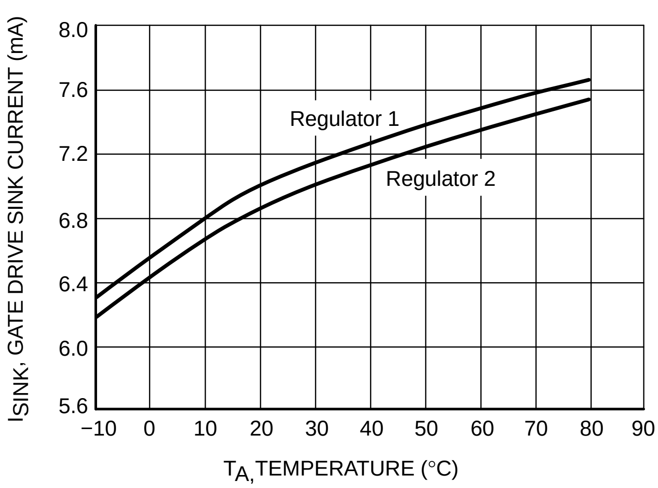


Figure 16. Gate Drive Sink Current vs. Ambient Temperature

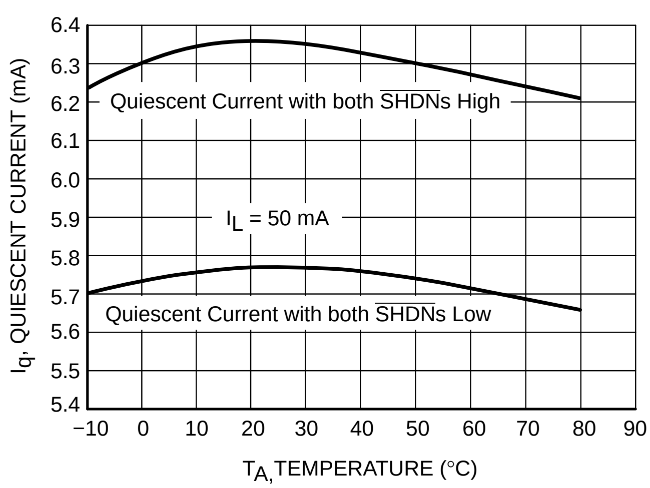


Figure 17. Quiescent Current vs. Ambient Temperature

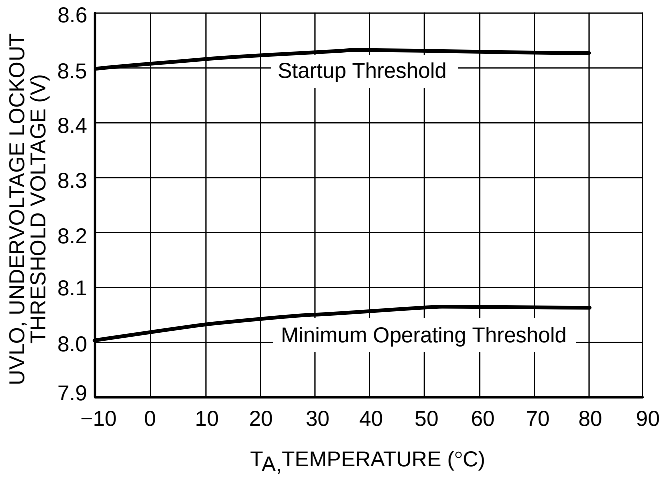


Figure 18. Undervoltage Lockout Threshold vs. Ambient Temperature

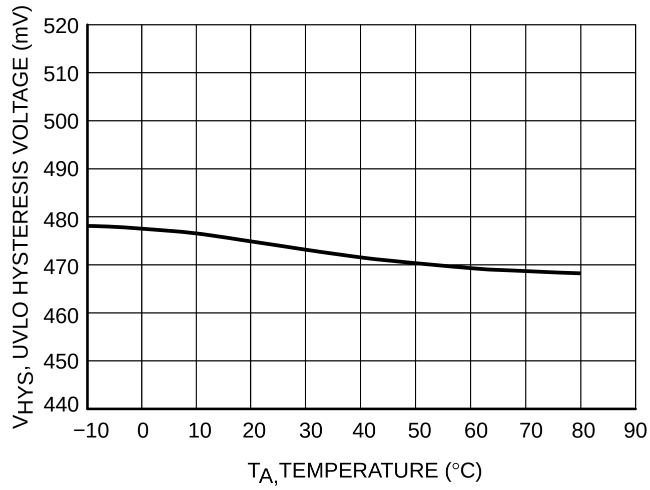


Figure 19. UVLO Hysteresis Voltage vs. Ambient Temperature

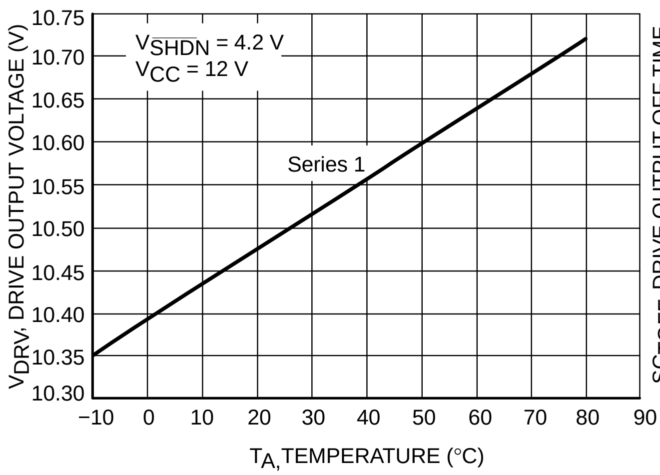


Figure 20. Regulator 2 Maximum Gate Voltage vs. Ambient Temperature

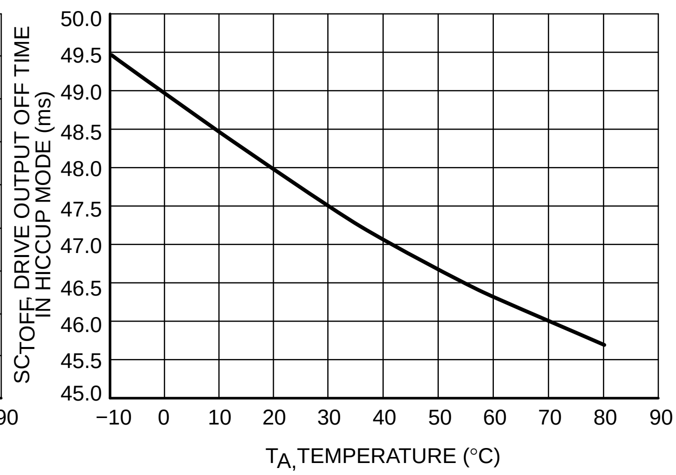


Figure 21. Drive Output Off Time in Hiccup Mode vs. Ambient Temperature

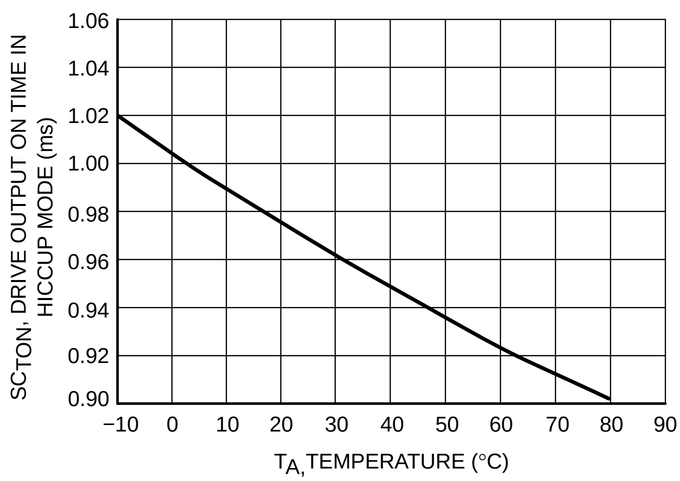


Figure 22. Drive Output On Time in Hiccup Mode vs. Ambient Temperature

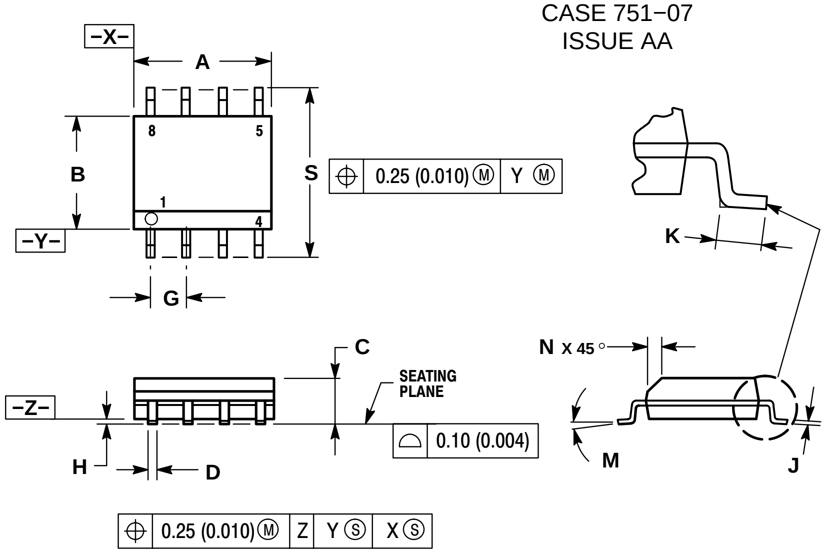
ORDERING INFORMATION

Device	V_{out1}	V_{out2}	Package	Shipping†
MC33567D−1	1.818 V	1.515 V or V_{in}*	SO−8	98 Units/Rail
MC33567D−1R2	1.818 V	1.515 V or V_{in}*	SO−8	2500/Tape & Reel
MC33567D−1R2G	1.818 V	1.515 V or V_{in}*	SO−8 (Pb−Free)	2500/Tape & Reel
MC33567D−2	2.525 V	2.525 V	SO−8	98 Units/Rail
MC33567D−2R2	2.525 V	2.525 V	SO−8	2500/Tape & Reel
MC33567D−3	2.300 V	1.200 V	SO−8	98 Units/Rail
MC33567D−3R2	2.300 V	1.200 V	SO−8	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*While on bypass mode.

PACKAGE DIMENSIONS

SO−8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751−07
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDAARD IS 751−07

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

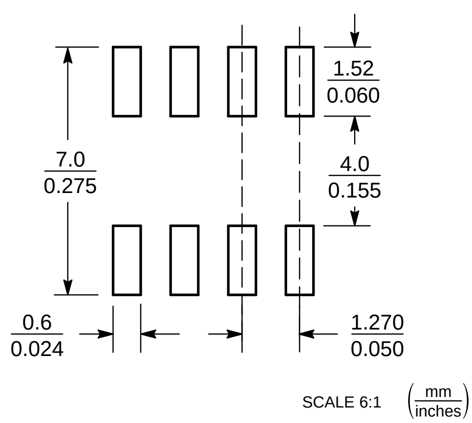


Figure 23. SO−8

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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